Design of Databus Charge Recovery Mechanism

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Abstract

We present a design for a charge recovery databus. Previous works have laid the groundwork for our design, presenting the theory that would make adiabatic circuit techniques useful. During a shorting period, the charge is transferred from the falling bit-lines to precharge the rising bit-lines while both the sender and the receiver are off.

We simulate this 8-bit charge recovery bus with data based on realistic benchmarks. The power savings average 20% over typical on-chip and off-chip bus capacitances. The savings increase with larger bus capacitances and longer shorting times. The overhead of the control circuitry is estimated at 3.6% of the total power consumption.

1 Introduction

In the past several years, circuit power dissipation has become an important element of VLSI design. Due to increasing die sizes and the physical limitation of wire scaling, interconnect structures are becoming one of the limiting factors in power and speed performance. Larger circuits require longer wires due to the connectivity requirements in design blocks beyond 100,000 gates [5]. Longer wires have more capacitance, forcing the driving devices to consume more power. A simple bus is one such structure that may not be suitable for low power design.

The power dissipation on a bus line can be reduced by applying adiabatic circuit design techniques. Part of the charge $Q = CV$ on a large capacitive load may be reused to lower the required current from V_{DD} during switching. Thus, in a databus, the charge from falling bit-lines can be used to precharge the rising bit-lines. After the next values of the databus become known, this technique requires some shorting time to accomplish the charge sharing.

For a traditional simple bus, the energy required for every bus cycle is

$$E = NCV\Delta V = NQV$$

where N is the number of rising bit-lines and Q is the charge needed for one bus line. With a charge recovery mechanism, the energy required to place the data onto the bus becomes

$$E = (NQ - Q_r)V$$

where Q_r is the total charge being reused on the bus [2]. Q_r is the charge that is transferred from the falling bit-lines to the rising bit-lines This reusable charge is proportional to $\frac{M}{N+M}$ with N rising bit-lines and M falling bit-lines.

In this paper, we will use the theoretical ideas presented in [1] and [2] to design a practical layout of the charge recovery mechanism. In addition to low power, we consider the speed factors affecting the performance of our circuit. We simulate the energy consumed by the charge recovery design and compare it to that of a simple databus design. Overall, it is found that the power savings of the charge recovery bus increase with larger bus capacitances, although longer shorting times are required to completely finish the charge transfers.

In the next section, we will will discuss the implementation of the charge recovery mechanism and the design issues addressed when forming a layout. In section 3, we present the tools and benchmarks used to test our design. The results are discussed in section 4. Finally, section 5 draws some conclusions from our work.

2 Implementation

During the charge transfer process, both the sender and the receiver buffers must tri-state. [2] proposes multiple charge transfers for most efficient charge sharing, involving multiple charge sharing cycles that need to be initiated on the bit lines of a bus. However, we use one shorting line in our design due to circuit overheads and speed concerns. The result is a single charge transfer involving multiple transitioning bus lines. Figure 1 shows the overview of the charge recovery bus. Four bus lines are shown, along with sending hardware and receiving buffers. The sending hardware constitutes the sending buffer, the switch, and the control needed to activate the switch.

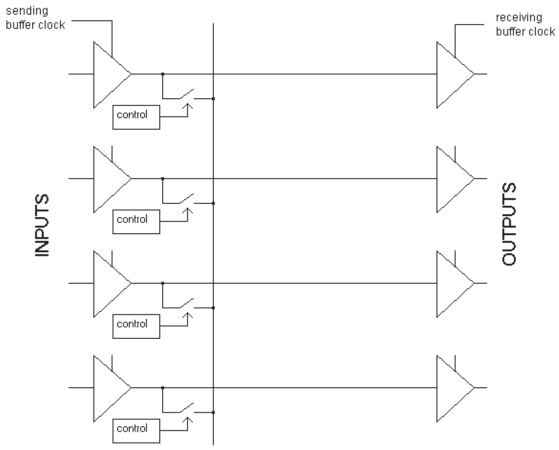

Figure 1: Overview of the charge recovery mechanism

Due to the control circuitry involved, the sending hardware becomes slightly more complicated. However, the comparative size of the drivers used to drive large capacitative loads makes the size of control circuitry seem like a minor addition. A five-stage sending buffer scaled up by a constant factor of 4 is used to drive the typical on-chip capacitances of 5pF to 10pF and an off-chip capacitance of 20pF [4]. Figure 2 shows the corresponding charge recovery hardware added to the buffer of a single bus line. A transmission gate is used as a switch to short the bus line to the common shorting line.

The XOR gate determines if the bus line will transition by looking at the previous bus state

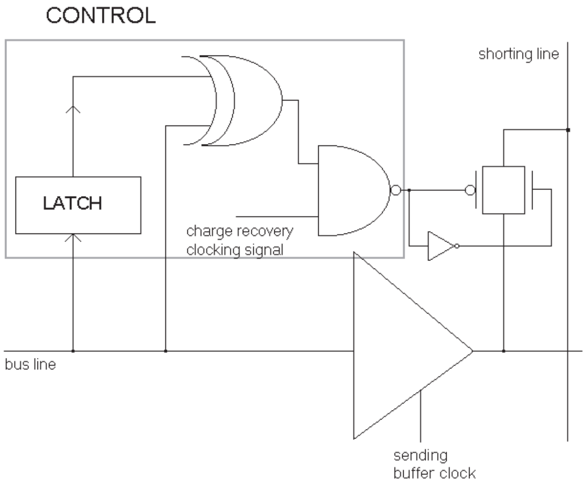

Figure 2: Design of control circuitry for the charge recovery bus

and the next bus state. If the value is transitioning, the transmission gate is enabled, connecting the bus line to the shorting line. A clocking signal is necessary to guarantee that the lines are shorted only when all the input and output buffers are tri-stated. To speed up the charge sharing time without large adverse effects on power savings, the size of the transmission gate is increased 8 times the minimal size.

3 Simulation

An 8-bit charge recovery bus and an 8-bit simple bus were used in the simulations. Both circuits were designed with 0.25μm, 3.3V technology using the Micro Magic toolset [6]. The simple bus consisted of a sending buffer and a receiving buffer, without the switch and the control of the charge recovery bus.

3.1 Test Bench

We generated an input sequence consisting of 30 datasets for our simulations. The sequence was constrained by the average bit transitions per memory access and the average bias of the Mediabench benchmark set [3]. The bias is a measure that captures the transition balance of a benchmark.

$$Bias = \left[\sum_{all\ transitions} |N - M| \right] * \frac{1}{total\ transitions}$$

where N is the number of rising bit-lines and M is the number of falling bit-lines [1]. The bus capacitances considered were 20pF, 10pF, and 5pF, representing the range of on-chip bus capacitances likely to benefit from a charge recovery scheme. Three different shorting times were tested for each of the bus capacitances. The times were determined from the plots of voltage vs. time on the bus lines. A sample plot is shown in Figure 3, obtained using HSPICE simulations. This plot was used to determine the various shorting times for the 20pF bus lines. The voltage on the bus line approaches 1.65 V (3.3/2 V).

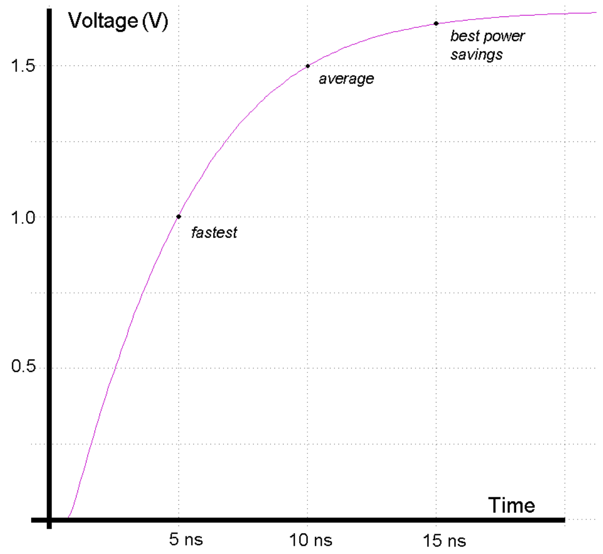

Figure 3: Sample plot of a bus line during the shorting period.

The cases considered were:

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1. Fastest Case:         charge transfer is
                         60% complete
2. Average Case:         good balance between
                         power savings and speed,
                         charge transfer is
                         90% complete
3. Best Power Savings:   charge transfer is
                         97% complete
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3.2 Clock Signals

Three non-overlapping clock signals were used for the charge recovery bus. These precautions were taken to avoid a floating bus and unnecessary switching currents. For the simple bus, a single clock signal to activate the receiver was necessary. Figure 4 demonstrates the clock signals of both simulation cases. These clock signals may be generated locally from a global clock with minimal overhead.

In the charge recovery circuit simulations, the shorting phase occurred right after the next state of the databus became known and was controlled by the charge recovery clock. Then, following the charge transfers, the sending buffer was turned on by the sending buffer clock, placing the values onto the bus lines. Finally, the receiving buffer was turned on by the receiving buffer clock, allowing the output device of the bus to read the data. In a practical scenario, the period of the charge recovery case may be reduced to a shorting phase and a bus activation phase.

In the simple bus circuit simulations, the next state of the databus was passed directly to the bus lines, keeping the sending buffer on at all times. Then, the receiving device reads the data once the receiving buffer is turned on.

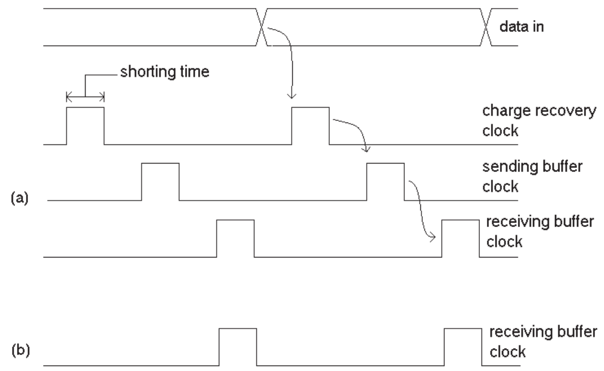

Figure 4: Clock signals for (a) charge recovery bus, and (b) simple bus

4 Results

In this section, we discuss the energy consumption of the charge recovery bus and compare it to the simple bus. Results of the simulations are shown in Table 1. The times represent the length of the shorting stage in the charge recovery bus. The clock periods of the simple bus cases were kept the same as the corresponding charge recovery cases, as shown in Figure 4.

As expected, the energy savings rise with larger bus capacitances. This effect occurs due to the increased charge that is transferred during a shorting period. With lower capacitance

	Fastest	Average	Best Savings
20pF bus	5ns	10ns	15ns
Charge Rec.	8.32mW	3.85mW	2.50mW
Simple	9.73mW	4.87mW	3.24mW
% Savings	17.0%	26.6%	29.5%
10pF bus	3ns	6ns	8ns
Charge Rec.	8.74mW	4.11mW	3.05mW
Simple	9.77mW	4.89mW	3.67mW
% Savings	11.8%	19.1%	20.3%
5pF bus	2ns	4ns	5ns
Charge Rec.	9.29mW	4.46mW	3.55mW
Simple	10.09mW	5.06mW	4.05mW
% Savings	8.6%	13.5%	14.1%

Table 1: Average Power Consumed by the Charge Recovery Bus and the Simple Bus

buses, the power consumed by the control circuitry is of greater significance, reducing the gains of charge sharing.

The best power savings of 29.5% occur with a bus capacitance of 20pF and the shorting time of 15ns. Since the shorting time may be too long for the required application, the power savings could be traded off for speed by either using the average case or by increasing the size of the transmission gate further for faster charge transfer. For all bus capacitances, the power savings from the average case tend to be close to their respective best power savings case.

Additional simulations were necessary to demonstrate the amount of power consumed by the control circuitry of the charge recovery mechanism. Table 2 shows the results of two simulations using a 0pF bus.

0pF bus	2ns	10ns
Charge Recovery	5.6034mW	1.1239mW
Simple	5.4081mW	1.0828mW
% Overhead	3.5%	3.7%

Table 2: Average Power Consumed by the Charge Recovery Bus and the Simple Bus

The results show that the charge recovery control circuitry uses an extra 3.6% of power than a simple bus. Thus, the extra power consumed demonstrates that the number of transistors used by the charge recovery mechanism is minimal compared to the bus driver itself. Still, the overhead may be especially noticeable for datasets containing a low number of transitions per access or a high bias.

The charge recovery scheme drastically reduces the maximum power consumed by a databus. In a simple bus, the maximum power consumption occurs when a significant number of bus lines are transitioning. In a charge recovery bus, during the same case, the rising bit-lines receive the reusable charge from the falling bit-lines, reducing the power consumed at that time. The only case when the charge recovery bus may consume a large amount of power is when all the transitioning bus lines are rising, with no falling bit-lines to share the charge.

Our experiments with shorting variable number of bit-lines of variable distance apart for the 8-bit and a 16-bit buses show no significant change in the time factor of the voltage vs. time plots. In a wider bus, as extra capacitances, in the form of bit lines, are connected to the shorting line during a charge sharing cycle, extra transmisison gates, which act as parallel resistors, are added as well. Therefore, the RC time-constant remains the same for every clock cycle.

In a practical design application, faster transition times may be desired for the charge recovery bus. The main bottleneck regarding speed in our design is the transmission gate that shorts a bus line to the common shorting line. By increasing the transmission gate size further, a portion of the power savings may be sacrificed for a significant increase in speed. Also, different circuitry could be used in the design of a switch for faster buses, a topic for future work in the area of charge recovery.

5 Conclusions

Our simulations use data transcribed from realistic benchmarks and bus coding techniques. The data sequence averages 2 bit transitions per memory access. With a larger bus, like 16-bit or 32-bit, the number of bit transitions per memory access is likely to increase proportionally. Therefore, the amount of available charge to be transferred would increase as well, leading to greater power savings.

Our charge recovery design produces average energy savings of 20% across typical on-chip and off-chip bus capacitances. Additional savings may be produced by combining our design with other low power techniques. Also, it may be possible to balance the number of rising bit-lines and the number of falling bit-lines for each clock cycle before sending the data to the bus.

Our design uses the ideas of previous works [2] and [1] to create a practical implementation of charge recovery circuit techniques. We showed that the savings increase with greater shorting times and with larger bus-line capacitances. The power overhead is 3.6%, increasing in significance with lower capacitances.

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